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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/424,544	INO ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2008 and 26 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-29,31,37 and 43-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-29,31,37 and 43-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of ***Species II (i.e., claims 49-70)*** in the reply filed on ***11 February 2008*** is acknowledged. The traversal is on the grounds:

(A) "*A Continued Prosecution Application (CPA) Request Transmittal was filed on February 26, 2003 along with a Request for Reconsideration. 37 C.F.R. § 1.53(d)*" (see page 2 of the election filed 11 February 2008).

This is not found persuasive because the instant application remains a national stage entry of PCT/JP99/01441.

Furthermore, even under the principles of US restriction practice, the instant invention demands restriction to claims directed to plural patentably distinct species.

The examiner respectfully notes that over the course of fourteen pages of arguments against the restriction (mailed 25 January 2008), the Applicant does not once dispute the clear fact that the instantly claimed invention includes multiple distinct, independent, and mutually exclusive species.

Two examples (there are also other sub-species pending -- e.g., **the horizontal scanning inversion driving technique** of claim 62 versus **the dot scanning inversion driving technique** of claim 63 -- still being claimed beyond the following two species):

Species I, drawn to the first inventive embodiment wherein a liquid crystal display comprising a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit, **the quantity of said general driver circuit output terminals being different than the quantity of said remainder driver circuit output terminals** (e.g., see claims 25-29, 31, 37, 43-48, and 71-78, fig. 5, and page 13, line 6 - page 15, line 9 of the specification); and

Species II, drawn to a liquid crystal display comprising a plurality of driver circuits, each of said plurality of driver circuits having a plurality of driver circuit output terminals, **the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits** (e.g., see claims 49-70, fig. 6, and page l 5, line 10 - page 18, line 19 of the specification).

These are two clearly mutually exclusive, distinct, and independent species. The Applicant does not dispute this fact. The Applicant's silence on this matter is respectfully taken as a concession of the presence of multiple mutually exclusive, distinct, and independent species in the instant claims.

(B) "*In response to these assertions, attention is drawn to the Petition under 37 C.F.R. §1.i44 filed on February 27, 2002*" (see page 4 of the election filed 11 February 2008).

This is not found persuasive because the Applicant has submitted at least nine claim amendment filings since 27 February 2002. The vast majority of currently pending claims (claims 43-78) did not even exist on the date of 27 February 2002. There are only two independent claims at present. Independent claim 25 is newly amended (as of 26 October 2007)

with brand new, unexamined subject matter. Independent claim 49 did not exist on the date of 27 February 2002. None of the currently elected claims (i.e., claims 49-70) existed on 27 February 2002.

Most of the special technical features argued by the Applicant back in 27 February 2002 (and repeated in the most recent election) are no longer even being claimed. Most of the 27 February 2002 argued claims have since been canceled. The old restriction requirement of 17 August 2001 does not remotely resemble the basis for the current restriction requirement. And the Applicant's arguments from 27 February 2002 are not commensurate in scope with presently pending claim language.

The examiner is not attempting to reintroduce an old restriction requirement based on long since canceled and amended claims. The Applicant's own amendments and arguments over the course of the last six years (since 27 February 2002) have resulted in an increasingly burdensome search and examination, and have persuaded the examiner that restriction is now appropriate and required.

The currently claimed Species I & II (listed above) do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, the species lack the same or corresponding special technical features for the following reasons:

Any international application must relate to one invention only or to a group of inventions so linked as to form a single general inventive concept (see MPEP 1850). As demonstrated by the "X" and "Y" references on the International Search Report, at least one claim of the application does not avoid the prior art, therefore, the special technical feature of the

application is anticipated by or obvious in view of the prior art. Consequently, the inventions listed above do not relate to a single general inventive concept under PCT Rule 13.1.

Furthermore, the species are independent or distinct because the species do not overlap in scope, i.e., are mutually exclusive; the species are not obvious variants; and the species each have a materially different design, mode of operation, function, and effect. The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Moreover, the examiner respectfully points out that all the instantly pending claims stand rejected under prior art grounds. Therefore, clearly, the instant application does not avoid the prior art and therefore the special technical feature of the application is anticipated by or obvious in view of the prior art. Restriction is thereby fully proper and appropriate.

(C) "*Because the features found within the claims have been previously acted upon on merits within the Office Actions prior to the Restriction Requirement of January 25, 2008, the*

search and examination of an entire application can be made without serious burden" (see page 8 of the election filed 11 February 2008).

This is not found persuasive because the Applicant's divergent arguments (for each claimed species) and divergent claim amendments clearly evidence the increasing search and examination burden on the examiner. The Applicant has two sets of inventions being prosecuted in two completely different ways. The two claimed species each feature completely different subject matter, structures, operations, limiting equations and variables. The Applicant's most recent response (filed 26 October 2007) completely overhauls one species (independent claim 25) via amendments; while leaving the other species (claim 49) untouched. The Applicant presents entirely different arguments for each species. The art that the examiner relies upon is different for each independent and distinct species. This office action is nearly sixty pages in length due to the presence of multiple distinct and independent inventions.

The most recent claim amendment (filed 26 October 2007) adds twelve hitherto unexamined claims, dramatically amends one of the independent species claims and completely rewrites three other dependent claims.

If the Applicant continues to insist that all the distinct and independent inventions be examined simultaneously, due to the overwhelmingly undue search and examination burden, the examiner cannot be certain that the best prior art will be located for each claimed species, rendering any potentially issued patent suspect.

The examiner respectfully notes that the instant US application has been granted priority to two separate and distinct Japanese patent applications (JP 10/241392 and JP 10/76813).

The examiner also respectfully notes that the Applicant found it necessary to seek two separate and distinct European patents (EP 1755105 A2 and EP 1069457 A1) based on the same specification.

Apparently, the Applicant believes the distinct and independent species of the instant invention constitute a search and examination burden everywhere expect in the United States.

By all rights, ***claims 25-29, 31, 37, 43-48, and 71-78*** should be withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to nonelected Species II, there being no allowable generic or linking claim. With the Applicant timely traversing the restriction (election) requirement in the reply filed on 11 February 2008.

2. Although the examiner does not find the Applicant's traversal arguments persuasive (for at least all the reasons listed above), purely as a courtesy to the Applicant, the examiner has rejected all the pending claims (even the ones drawn to nonelected Species I) below.

Again, solely as a courtesy to the Applicant, the restriction requirement (mailed 25 January 2008) is hereby withdrawn. All the pending claims 25-29, 31, 37 and 43-78 have been search, examined, and rejected.

Although the restriction requirement has been withdrawn; the examiner respectfully maintains (for at least all the reasons listed above) the claims include distinct, independent, and mutually exclusive species which do not relate to a single general inventive concept and present an undue burden to search and examine.

The Applicant is respectfully requested to reconsider the restriction traversal filed 11 February 2008, and to consider filing ***claims 25-29, 31, 37, 43-48, and 71-78*** (drawn to nonelected Species I) in a separate Divisional application; such that the examiner can better guarantee the most complete search and examination.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

4. The drawings were received on 4 February 2004. These drawings are acceptable.

5. The lengthy number of drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 25-29, 31, 37, 43-48, and 67-78 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***said plurality of driver circuits***" (in line 18). It would be unclear to one having ordinary skill in the art whether "***said plurality of driver circuits***" (in line 18) is intended to refer back to the earlier claimed "***a plurality of driver circuits***" (in line 6); or rather intended to refer back to the earlier claimed "***at least one general driver circuit***" (in line 6); or rather intended to refer back to the earlier claimed "***one remainder driver circuit***" (in line 7); or rather intended to refer back to some undefined combination of the aforementioned "***driver circuits***".

An omitted structural cooperative relationship results from the claimed subject matter: "***providing another signal potential to another of said plurality of signal lines***" (in line 14). It would be unclear to one having ordinary skill in the art what the "*signal potential*" and "*signal line*" are intended respectively to be "*another*" (i.e., "*additional*") to. Does the remainder driver circuit provide more than one signal potential to multiple signal lines?

10. Claim 25 recites the limitations:

"***the quantity of said remainder driver circuit output terminals***" (in line 16);

"***the quantity of said plurality of signal lines***" (in line 17);

"***the quantity of said general driver circuit output terminals***" (in line 17); and

"***the quantity of said plurality of driver circuits***" (in line 18).

There is insufficient antecedent basis for these limitations in the claim. A "*quantity*" may represent a particular or indefinite amount of anything. The present claim language provides no guidance for what is meant by "*the quantity*." It would be unclear to one having ordinary skill in the art whether the "*quantity*" is intended to represent the "*number*" of terminals, lines, and/or circuits respectively present in the claimed invention; or rather whether the "*quantity*" is intended to represent the "*weight*" of the respective terminals, lines, and/or circuits; or rather whether the "*quantity*" is intended to represent the "*dimensions*" (length, width, height, etc.) of the respective terminals, lines, and/or circuits.

11. Claim 25 recites the limitation "***horizontal***" (in lines 8 and 12). There is insufficient antecedent basis for this limitation in the claim. The claim defines no dimensional planes. It would be unclear to an artisan what such a "***horizontal***" limitation is intended to be relative to. What claim element, if any, defines the horizontal plane?

12. Claims 26-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of

elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results for the claimed subject matter: "***a display***" (in line 1 of each dependent claim). It would be unclear to one having ordinary skill in the art whether "***a display***" in each respective dependent claim is intended to refer back to the earlier claimed "***a liquid crystal display***" (in independent claim 25, line 1); or rather whether "***a display***" in each respective dependent claim is intended represent a separate and distinct display from the earlier claimed "***a liquid crystal display***" (in independent claim 25, line 1). Does the display of each of the dependent claims even need to be a liquid crystal display? Or can it be any type of display (e.g., CRT, EL, FET, etc.)?

13. Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***said plurality of driver circuits***" (in line 2). It would be unclear to one having ordinary skill in the art whether "***said plurality of driver circuits***" is intended to refer back to the earlier claimed "***a plurality of driver circuits***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***at least one general driver circuit***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***one remainder driver circuit***" (in claim 25, line 7); or rather intended to refer back to some undefined combination of the aforementioned "***driver circuits***".

14. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a source/drain***" (in line 3). It would be unclear to one having ordinary skill in the art whether this limitation is intended to mean "***a source or a drain***"; rather intended to mean "***a source and a drain***".

15. Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a surplus connecting region that does not contribute to said display portion does not occur on the said display***" (in line 1). It would be unclear to one having ordinary skill in the art whether or not "***a surplus connecting region***" is an element of the claimed invention. It's further unclear what if anything such a region is intended to be connecting while it's not contributing or occurring.

16. The term "***does not contribute***" in claim 31, line 2 is a relative term which renders the claim indefinite. The term "***contribute***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would

not be reasonably apprised of the scope of the invention. One artisan's impression of a "*contribution*" is just as likely to be another artisan's idea of a detriment.

17. Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***said plurality of driver circuits***" (in line 2). It would be unclear to one having ordinary skill in the art whether "***said plurality of driver circuits***" is intended to refer back to the earlier claimed "***a plurality of driver circuits***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***at least one general driver circuit***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***one remainder driver circuit***" (in claim 25, line 7); or rather intended to refer back to some undefined combination of the aforementioned "***driver circuits***".

An omitted structural cooperative relationship results from the claimed subject matter: "***that is***" (in line 5) and "***supplied***" (in line 6). It would be unclear to one having ordinary skill in the art what the respective subject(s) of "***that is***" and "***supplied***" are intended to be. The signal potential? The color?

18. Claim 37 recites the limitation "***a de-multiplexed signal potential***" (in line 3). There is insufficient antecedent basis for this limitation in the claim. It would be unclear to one having ordinary skill whether or not a de-multiplexer is a claim element.

19. Claim 43 recites the limitation "***a third primary color***" (in line 2). There is insufficient antecedent basis for this limitation in the claim. Base claim 37 only recites two primary colors. It would be unclear to one having ordinary skill whether or not a third primary color exists as a claim element.

20. Claim 45 recites the limitation "***the sum total***" (in line 1). There is insufficient antecedent basis for this limitation in the claim.

21. Claim 45 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines***" (in line 2).

It would be unclear to one having ordinary skill in the art whether the "***general driver circuit output terminals***" are identical to the earlier claimed "***plurality of general driver circuit output terminals***" (in independent claim 25, line 9); or rather whether they are distinct and different from the earlier claimed "***plurality of general driver circuit output terminals***".

Moreover, it would be unclear to one having ordinary skill in the art how "***the sum total of general driver circuit output terminals and said remainder driver circuit output terminals***" can be "***equal to said plurality of signal lines***". Is that intended to mean the terminals and lines

are made out of the same material (i.e., equal materials)? Are these terminals/lines limitations identical or different from the "***quantities***" of terminals/lines recited in independent claim 25?

22. Claim 46 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***said plurality of driver circuits***" (in line 1). It would be unclear to one having ordinary skill in the art whether "***said plurality of driver circuits***" is intended to refer back to the earlier claimed "***a plurality of driver circuits***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***at least one general driver circuit***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***one remainder driver circuit***" (in claim 25, line 7); or rather intended to refer back to some undefined combination of the aforementioned "***driver circuits***".

23. Claim 47 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***an equal number***" (in line 2). It would be unclear to one having ordinary skill in the art what such a number is intended to be equal to.

Moreover, it would be unclear to one having ordinary skill in the art whether the "***general driver circuit output terminals***" are identical to the earlier claimed "***plurality of general driver***

circuit output terminals" (in independent claim 25, line 9); or rather whether they are distinct and different from the earlier claimed "***plurality of general driver circuit output terminals***".

24. Claim 48 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***said plurality of driver circuits***" (in line 1). It would be unclear to one having ordinary skill in the art whether "***said plurality of driver circuits***" is intended to refer back to the earlier claimed "***a plurality of driver circuits***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***at least one general driver circuit***" (in claim 25, line 6); or rather intended to refer back to the earlier claimed "***one remainder driver circuit***" (in claim 25, line 7); or rather intended to refer back to some undefined combination of the aforementioned "***driver circuits***".

An omitted structural cooperative relationship results from the claimed subject matter: "***driver integrated circuits***" (in line 2). It would be unclear to one having ordinary skill in the art what such circuits are intended to be integrated with.

An omitted structural cooperative relationship results from the claimed subject matter: "***which***" (in line 3). It would be unclear to one having ordinary skill in the art what the subject of "***which***" is intended to be. The substrate? The outside? The circuits?

25. Claims 67-70 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results for the claimed subject matter: "***a display***" (in line 1 of each dependent claim). It would be unclear to one having ordinary skill in the art whether "***a display***" in each respective dependent claim is intended to refer back to the earlier claimed "***a liquid crystal display***" (in independent claim 49, line 1); or rather whether "***a display***" in each respective dependent claim is intended represent a separate and distinct display from the earlier claimed "***a liquid crystal display***" (in independent claim 49, line 1). Does the display of each of the dependent claims even need to be a liquid crystal display? Or can it be any type of display (e.g., CRT, EL, FET, etc.)?

26. Claim 67 recites the limitation "***horizontal***" (in line 2). There is insufficient antecedent basis for this limitation in the claim. The claim defines no dimensional planes. It would be unclear to an artisan what such a "***horizontal***" limitation is intended to be relative to. What claim element, if any, defines the horizontal plane?

27. Claim 68 recites the limitations: "***one general driver horizontal shift register circuit of said plurality of driver circuits***" (in line 1) and "***another general driver horizontal shift register circuit of said plurality of driver circuits***" (in line 2). There is insufficient antecedent basis for these limitation in the claim.

28. Claim 69 recites the limitation "***horizontal***" (in line 2). There is insufficient antecedent basis for this limitation in the claim. The claim defines no dimensional planes. It would be unclear to an artisan what such a "***horizontal***" limitation is intended to be relative to. What claim element, if any, defines the horizontal plane?

29. Claim 70 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a digital/analog converting circuit***" (in line 2). It would be unclear to one having ordinary skill in the art whether this limitation is intended to mean "***a circuit converting digital signals to analog signals***"; rather intended to mean "***a circuit converting either digital or analog signals***".

30. Claim 71 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***one general driver horizontal shift register circuit of said plurality of driver circuits***" (in line 1) and "***another general driver horizontal shift register circuit of said plurality of driver circuits***" (in line 2). It would be unclear to one having ordinary skill in the art whether the "***general driver horizontal shift register circuit***" are intended to be identical to the earlier claimed "***a general driver horizontal shift register circuit***" (in claim 25, line 8); or rather intended to be

distinct and different from to the earlier claimed "***a general driver horizontal shift register circuit***" (in claim 25, line 8).

31. Claim 72 recites the limitation "***horizontal***" (in line 2). There is insufficient antecedent basis for this limitation in the claim. The claim defines no dimensional planes. It would be unclear to an artisan what such a "***horizontal***" limitation is intended to be relative to. What claim element, if any, defines the horizontal plane?

32. Claim 73 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a digital/analog converting circuit***" (in line 3). It would be unclear to one having ordinary skill in the art whether this limitation is intended to mean "***a circuit converting digital signals to analog signals***"; rather intended to mean "***a circuit converting either digital or analog signals***".

33. Claim 74 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***sampling switches***" (in line 1). It would be unclear to one having ordinary skill in the art whether this limitation is intended to be identical to the earlier claimed "***sampling switches***" (in

claim 73, line 2); or rather intended to be distinct and different from to the earlier claimed "***sampling switches***".

34. Claim 74 recites the limitation "***input digital image data***" (in line 2). The lack of a grammatical article (such as "***a***" or "***a plurality of***" or "***the***" or "***said***") preceding the limitation renders it unclear whether the claim is establishing a new element; or instead referring back to some preestablished limitation. For example, it would be unclear to an artisan whether a single element of "***data***" is being claimed; or rather whether a plurality of "***data***" elements are being claimed.

35. Claim 74 recites the limitation "***horizontal***" (in line 2). There is insufficient antecedent basis for this limitation in the claim. The claim defines no dimensional planes. It would be unclear to an artisan what such a "***horizontal***" limitation is intended to be relative to. What claim element, if any, defines the horizontal plane?

36. Claim 75 recites the limitation "***digital data***" (twice in line 2). The lack of a grammatical article (such as "***a***" or "***a plurality of***" or "***the***" or "***said***") preceding the limitation renders it unclear whether the claim is establishing a new element; or instead referring back to some preestablished limitation. For example, it would be unclear to an artisan whether a single element of "***data***" is being claimed; or rather whether a plurality of "***data***" elements are being claimed.

Additionally, it would be unclear to an artisan whether "***digital data***" listed twice in line 2 refers to the same identical data; or rather is intended to refers to distinct and different data.

37. Claim 76 recites the limitation "***digital data***" (in line 2). The lack of a grammatical article (such as "***a***" or "***a plurality of***" or "***the***" or "***said***") preceding the limitation renders it unclear whether the claim is establishing a new element; or instead referring back to some preestablished limitation. For example, it would be unclear to an artisan whether a single element of "***data***" is being claimed; or rather whether a plurality of "***data***" elements are being claimed.

38. Claim 76 recites the limitation "***digital data boosted***" (in line 2). There is insufficient antecedent basis for this limitation in the claim. It would be unclear to an artisan whether or not a pre-boosted data element is part of the claimed invention.

39. Claim 76 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***digital data boosted by said general driver level shifter by an amount of one horizontal period***" (in line 2). It would be unclear to one having ordinary skill in the art how a time period is even capable of "boosting" digital data. Digital data by it's very definition can only take one of two values.

40. Claim 76 recites the limitation "***horizontal***" (in line 3). There is insufficient antecedent basis for this limitation in the claim. The claim defines no dimensional planes. It would be

unclear to an artisan what such a "***horizontal***" limitation is intended to be relative to. What claim element, if any, defines the horizontal plane?

41. Claim 77 recites the limitation "***digital data***" (in line 2). The lack of a grammatical article (such as "***a***" or "***a plurality of***" or "***the***" or "***said***") preceding the limitation renders it unclear whether the claim is establishing a new element; or instead referring back to some preestablished limitation. For example, it would be unclear to an artisan whether a single element of "***data***" is being claimed; or rather whether a plurality of "***data***" elements are being claimed.

42. Claim 77 recites the limitation "***horizontal***" (in line 2). There is insufficient antecedent basis for this limitation in the claim. The claim defines no dimensional planes. It would be unclear to an artisan what such a "***horizontal***" limitation is intended to be relative to. What claim element, if any, defines the horizontal plane?

43. Claim 77 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***which***" (in line 2). It would be unclear to one having ordinary skill in the art what the subject of "***which***" is intended to be. The period? The data?

44. Claim 78 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a digital/analog converting circuit***" (in line 3). It would be unclear to one having ordinary skill in the art whether this limitation is intended to mean "***a circuit converting digital signals to analog signals***"; rather intended to mean "***a circuit converting either digital or analog signals***".

Claim Rejections - 35 USC § 102/103

45. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

46. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

47. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

48. Claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 102(b) as anticipated by ***Takeda et al (US 4,825,203 A)***.

49. Claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 102(b) as anticipated by ***Hirai (US 5,440,304 A)***.

50. Or, in the alternative, claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** in view of ***Hirai (US 5,440,304 A)***.

Regarding claim 25, Takeda discloses a liquid crystal display [e.g., Fig. 2, 11] (see the entire document, including the Abstract) comprising:

a display portion [e.g., Fig. 2, 11], said display portion having a plurality of gate lines [e.g., Fig. 2, 11-a], a plurality of signal lines [e.g., Fig. 2, 11-b] and a plurality of pixels [e.g., Fig. 2, 11-c],

a pixel [e.g., Fig. 2, 11-c] of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines (see the entire document, including Fig. 2); and

a plurality of driver circuits [e.g., Figs. 1(A) & 2, 13, q_1-q_N], said plurality of driver circuits including at least one general driver circuit [e.g., Figs. 1(A), q_1, q_2, and q_3] and one remainder driver circuit [e.g., Figs. 1(A), q_{n-1} and q_n],

each said at least one general driver circuit having a general driver horizontal shift register circuit [e.g., Fig. 1(A), 31] and a plurality of general driver circuit output terminals [e.g., Fig. 1(A), at 36-1, 36-2, and 36-3], a general driver circuit output terminal [e.g., Fig. 1(A), at 36-1, 36-2, or 36-3] of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines [e.g., Fig. 1(A), Q1, Q2, or Q3],

said remainder driver circuit having a remainder driver horizontal shift register circuit [e.g., Fig. 1(A), 31] a plurality of remainder driver circuit output terminals [e.g., Fig. 1(A), 36-(N-1) and 36-N], a remainder driver circuit output terminal [e.g., Fig. 1(A), 36-(N-1) or 36-N] of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines [e.g., Fig. 1(A), Q_{N-1} or Q_N],

the quantity [e.g., 2] of said remainder driver circuit output terminals being defined as (S - (OP * (DC-1))), "S" being the quantity [e.g., 5] of said plurality of signal lines, "OP" being the quantity [e.g., 3] of said general driver circuit output terminals, and "DC" being the quantity [e.g., 2] of said plurality of driver circuits, and

said quantity [e.g., 3] of said general driver circuit output terminals being different than said quantity [e.g., 2] of said remainder driver circuit output terminals [see the entire document, including Fig. 1(A) and Column 4, Lines 22-68 -- wherein S - (OP * (DC-1)) = 5 - (3 * (2-1)) = 5 - (3 * 1) = 5 - 3 = 2 = the quantity of remainder driver circuit output terminals = 2].

The instant claim nowhere expressly specifies that the general driver horizontal shift register circuit and the remainder driver horizontal shift register circuit must be different and distinct from one another. Therefore, an artisan would reasonably expect that a single generic

shift register circuit may be shared by both the general driver horizontal shift register circuit and the remainder driver horizontal shift register circuit of the instant invention.

Furthermore, the examiner takes official notice that one having ordinary skill in the art at the time of invention would recognize that Takeda's shift register circuit [e.g., Fig. 1(A), 31] is conventionally comprised by a series of distinct flip flops set up in a linear fashion which have their inputs and outputs connected together in such a way that the data [e.g., Fig. 1(A), D] are shifted down the line [e.g., Fig. 1(A); from q_1 to q_N] when the circuit is activated [e.g., Fig. 1(A), via clock signal Φ]. In such a manner, Takeda's shift register circuit [e.g., Fig. 1(A), 31] would conventionally have a first set of flip flops provided for the general driver circuitry [e.g., Figs. 1(A), outputting at q_1, q_2, and q_3] and a following second set of flip flops provided for the remainder driver circuitry [e.g., Figs. 1(A), outputting at q_{n-1} and q_n]. In such a manner, Takeda reads on the general driver horizontal shift register circuit and the remainder driver horizontal shift register circuit of the instantly claimed invention.

However, should it be shown that Takeda neglects teaching such general and remainder driver horizontal shift register circuits; Hirai discloses a liquid crystal display [e.g., Fig. 1, 26] comprising:

a display portion [e.g., Fig. 1, 26], said display portion having a plurality of gate lines, a plurality of signal lines [e.g., Fig. 1, Y] and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [e.g., Fig. 1; 18 and Figs. 3-5, 20], said plurality of driver circuits including at least one general driver circuit [e.g., Fig. 5, leftmost two 20 circuits] and one remainder driver circuit [e.g., Fig. 5, rightmost 20 circuit],

each said at least one general driver circuit having a general driver horizontal shift register circuit [e.g., Figs. 1 & 2; 11 and Fig. 3; 21] and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines [e.g., Figs. 3 & 5, Y_1-Y_{80}] (see the entire document, including Column 4, Line 15 - Column 5, Line 42),

said remainder driver circuit having a remainder driver horizontal shift register circuit [e.g., Figs. 1 & 2; 11 and Fig. 3; 21] a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines [e.g., Figs. 3 & 5, Y_1-Y_{16}],

the quantity [e.g., 16] of said remainder driver circuit output terminals being defined as (S - (OP * (DC-1))), "S" being the quantity [e.g., 176] of said plurality of signal lines, "OP" being the quantity [e.g., 80] of said general driver circuit output terminals, and "DC" being the quantity [e.g., 3] of said plurality of driver circuits, and

said quantity [e.g., 80] of said general driver circuit output terminals being different than said quantity [e.g., 16] of said remainder driver circuit output terminals (see the entire document, including Column 1, Line 5 - Column 2, Line 60).

Hirai also discloses the shift register circuit [e.g., Fig. 2, 11] is being comprised by a series of distinct flip flops [e.g., Fig. 2, FF_1-FF_{80}] set up in a linear fashion which have their inputs and outputs connected together in such a way that the data [e.g., Fig. 2, DI] are shifted down the line [e.g., Fig. 2, Y_1-Y_{80}] when the circuit is activated [e.g., Fig. 2, via clock signal CL2] (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Should it be shown that Hirai neglects teaching a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate such an active matrix type structure, so as to provide a light weight display having very good image quality, wide color gamut, and relatively fast response time. Moreover, as already detailed above, Takeda teaches such subject matter.

Takeda and Hirai are analogous art, because they are from the shared inventive field of using shift register circuitry to drive a liquid crystal display. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Hirai's integrated shift register circuitry to drive Takeda's liquid crystal display device, so as to use a conventional type of shift register and to eliminate the need for mixing serial data to be input with dummy data even if the necessary total of output bits cannot be divided by the number of output bits of a single IC.

It would have been obvious to one of ordinary skill in the art at the time of invention because all the claimed elements were known in the prior art and one skilled in the art could have

combined the integrated shift register circuitry as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known shift register circuit for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the technique for improving (by integrating the shift register circuitry) this particular class of LCD device was part of the ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

It would have been obvious to one of ordinary skill in the art at the time of invention, because this particular known shift register circuitry integration technique was recognized as part of the ordinary capabilities of one skilled in the art.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (e.g., integrating shift register circuitry). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

It would have been obvious to one of ordinary skill in the art at the time of invention, because design incentives or market forces provided a reason to make a shift register circuitry integration adaptation, and the invention resulted from application of the prior knowledge in a predictable manner.

Regarding claim 26, Takeda discloses one driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits [see the entire document, including Fig. 1(A)].

Hirai discloses one driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Regarding claim 27, Takeda discloses said plurality of pixels is arranged in a two-dimensional matrix shape (see the entire document, including Fig. 2).

Hirai discloses said plurality of pixels is arranged in a two-dimensional matrix shape (see the entire document, including Fig. 3).

Regarding claim 28, Takeda discloses said pixel of said plurality of pixels includes a transistor [e.g., Fig. 2, 11-d], a gate electrode [e.g., Fig. 2, at 11-a] of said transistor being electrically connected to said gate line, a source/drain [e.g., Fig. 2, at 11-b] of said transistor being electrically connected to said signal line (see the entire document, including Fig. 2; Column 2, Lines 56-68).

Hirai discloses said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Regarding claim 29, Takeda discloses said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns (see the entire document, including Fig. 2).

Hirai discloses said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Regarding claim 31, Takeda discloses a surplus connecting region [e.g., Fig. 2; 12, 13, & 15] that does not contribute to said display portion [e.g., Fig. 2, 11] does not occur on the said display (see the entire document, including Column 2, Line 56 - Column 3, Line 27).

Hirai discloses a surplus connecting region that does not contribute to said display portion does not occur on the said display (see the entire document, including Fig. 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 37, Takeda discloses an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch [e.g., Fig. 1(A), 32], said time-divisional switch providing a de-multiplexed signal potential to said signal line,

said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line (see the entire document, including Column 4, Lines 22-68).

Hirai discloses an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line (see the entire document, including Fig. 3; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 43, Takeda discloses said plurality of primary colors is a first primary color, a second primary color and a third primary color (see the entire document, including Column 2, Lines 55-68).

Hirai discloses said plurality of primary colors is a first primary color, a second primary color and a third primary color (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Regarding claim 44, Takeda discloses said quantity [e.g., 3] of general driver circuit output terminals is greater than said quantity [e.g., 2] of remainder driver circuit output terminals [see the entire document, including Fig. 1(A)].

Hirai discloses said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals (see the entire document, including Fig. 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 45, Takeda discloses the sum total of general driver circuit output terminals [e.g., 3] and said remainder driver circuit output terminals [e.g., 2] is equal to said plurality of signal lines [e.g., 5] [see the entire document, including Fig. 1(A)].

Hirai discloses the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines (see the entire document, including Fig. 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 46, Takeda discloses said plurality of driver circuits includes more than one said general driver circuit [see the entire document, including Fig. 1(A)].

Hirai discloses said plurality of driver circuits includes more than one said general driver circuit (see the entire document, including Fig. 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 47, Takeda discloses said each said general driver circuit has an equal number of general driver circuit output terminals [see the entire document, including Fig. 1(A)].

Hirai discloses said each said general driver circuit has an equal number of general driver circuit output terminals (see the entire document, including Fig. 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 48, Takeda discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Hirai discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (see the entire document, including Fig. 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 71, Hirai discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (see the entire document, including Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60).

Takeda discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Regarding claim 72, Hirai discloses said general driver horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (see the entire document, including Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42).

Takeda discloses said general driver horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Regarding claim 73, Hirai discloses said each said at least one general driver circuit has general driver sampling switches [e.g., Fig. 2, FF1-FF80], a general driver level shifter [e.g., Fig. 1, 23], a general driver data latch circuit [e.g., Fig. 1, 22], and a general driver digital/analog converting circuit [e.g., Fig. 1, 22] (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Takeda discloses said each said at least one general driver circuit has general driver sampling switches, a general driver level shifter, a general driver data latch circuit, and a general driver digital/analog converting circuit (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Should it be shown that Hirai neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Regarding claim 74, Hirai discloses sampling switches [e.g., Fig. 2, FF1-FF80] in said general driver sampling switches sequentially sample input digital image data in response to horizontal scanning pulses from said general driver horizontal shift register circuit (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Takeda discloses sampling switches in said general driver sampling switches sequentially sample input digital image data in response to horizontal scanning pulses from said general

driver horizontal shift register circuit (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Should it be shown that Hirai neglects teaching a digital data with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to use digital signals, so as to assure that all signals are at appropriate levels.

Regarding claim 75, Hirai discloses said general driver level shifter boosts digital data sampled by said general driver sampling switches to digital data of a liquid crystal driving voltage (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Takeda discloses said general driver level shifter boosts digital data sampled by said general driver sampling switches to digital data of a liquid crystal driving voltage (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Should it be shown that Hirai neglects teaching a digital data with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to use digital signals, so as to assure that all signals are at appropriate levels.

Regarding claim 76, Hirai discloses said general driver data latch circuit is a memory to accumulate digital data boosted by said general driver level shifter by an amount of one horizontal period (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Takeda discloses said general driver data latch circuit is a memory to accumulate digital data boosted by said general driver level shifter by an amount of one horizontal period (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Should it be shown that Hirai neglects teaching a digital data with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to use digital signals, so as to assure that all signals are at appropriate levels.

Regarding claim 77, Hirai discloses said general driver digital/analog converting circuit converts digital data of one horizontal period which is outputted from said general driver data latch circuit into an analog signal and outputs said analog signal (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Takeda discloses said general driver digital/analog converting circuit converts digital data of one horizontal period which is outputted from said general driver data latch circuit into an analog signal and outputs said analog signal (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Should it be shown that Hirai neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Regarding claim 78, Hirai discloses said remainder driver circuit has remainder driver sampling switches [e.g., Fig. 2, FF1-FF80], a remainder driver level shifter [e.g., Fig. 1, 23], a remainder driver data latch circuit [e.g., Fig. 1, 22], and a remainder driver digital/analog converting circuit [e.g., Fig. 1, 22] (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Takeda discloses said remainder driver circuit has remainder driver sampling switches, a remainder driver level shifter, a remainder driver data latch circuit, and a remainder driver digital/analog converting circuit (see the entire document, including Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Should it be shown that Hirai neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

51. Claims 49-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** in view of ***Lee (US 5,426,447 A)***.

Regarding claim 49, Takeda discloses a liquid crystal display [e.g., Fig. 2, 11] comprising:

a display portion [e.g., Fig. 2, 11], said display portion having a plurality of gate lines [e.g., Fig. 2, 11-a], a plurality of signal lines [e.g., Fig. 2, 11-b] and a plurality of pixels [e.g., Fig. 2, 11-c],

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and a plurality of driver circuits [e.g., Figs. 1(A) & 2, 13 & q_1-q_n] (see the entire document, including Column 2, Line 56 - Column 3, Line 27), each of said plurality of driver circuits having a plurality of driver circuit output terminals [e.g., Fig. 1(A), at 37],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line [e.g., Fig. 1(A), Q_1 to Q_N] of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (see the entire document, including Column 4, Lines 22-68).

Takeda does not expressly use the explicit term, "pixel" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion comprising a plurality of "pixels" is formed (see the entire document, including Column 1, Lines 18-30).

Takeda and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Lee's "pixel" terminology to describe Takeda's "display picture elements", so as to make use of common terminology in the art.

Regarding claim 50, Takeda discloses a plurality of time-divisional switches [e.g., Fig. 1(A), 32], said plurality of time-divisional switches receiving said signal potential from said

driver circuit output terminal and time-divisionally sending said received signal potential said signal line (see the entire document, including Column 4, Lines 22-68).

Regarding claim 51, Takeda discloses the quantity of said time-divisional switches is equal to 3 [see the entire document, including Fig. 1(A), 32] (see the entire document, including Column 4, Lines 22-68).

Regarding claim 52, Takeda discloses said quantity of said signal lines is different than said quantity of said driver circuit output terminals (see the entire document, including Fig. 1(A) and Column 4, Lines 22-68).

Regarding claim 53, Takeda discloses said quantity of said driver circuit output terminals is set to a power of 2 (see the entire document, including Fig. 1(A) and Column 4, Lines 22-68).

Regarding claim 54, although Takeda's Figures 1(A) and 2 render it readily apparent that the column electrode drive circuit [13] comprises driver ICs outside the display substrate [11], and although every material presently known to man possesses an inherent insulative capacity, and although it's arguable that the Takeda's LCD must feature at least one transparent substrate in order for a user to actually view a displayed image, Takeda does not expressly use the explicit term, "transparent insulating substrate" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion is formed (see the entire document, including Column 1, Lines 28-30).

Takeda and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Lee's transparent insulating glass substrate to form Takeda's liquid crystal display, so as to make it possible for users to actually view any displayed images.

Regarding claim 55, Takeda discloses a memory circuit [e.g., Fig. 1(A), 31] for temporarily storing data [e.g., Fig. 1(A), D] to be written into said plurality of driver circuits; and a control circuit [e.g., Fig. 2, 15] for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit (see the entire document, including Column 3, Lines 8-27 & Column 4, Lines 22-68).

Regarding claim 56, Takeda discloses a leading waveform and a trailing waveform of a signal output waveform [e.g., Fig. 1(B), C_R, C_G & C_B] of each of said plurality of driver circuits are symmetrical with respect to a time base (see the entire document, including Column 4, Lines 47-68).

Regarding claim 57, Takeda discloses a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period (see the entire document, including Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 58, Takeda discloses a leading time and a trailing time of each of said plurality of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches (see the entire document, including Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 59, Takeda discloses a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal Scanning period - the period of time selected by the time-divisional switches x 3) / 3 (see the entire document, including Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 60, Takeda discloses said plurality of driver circuits have a function to stop the operation of an output circuit of said plurality of driver circuits for said blanking period (see the entire document, including Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 61, Takeda discloses said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) [see the entire document, including Fig. 1(A), V_R, V_G & V_B] by diving to said time-divisional switches (see the entire document, including Column 4, Lines 22-46).

Regarding claim 62, Takeda discloses within a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the

second time is a line of green, and the signal line which is selected at the third time is a line of red [see the entire document, including Fig. 4(B); Row i+2 & Columns j, j+1 and j+2].

Regarding claim 63, Takeda discloses within a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue [see the entire document, including Fig. 5(B); Row i & Columns j, j+1 and j+2].

Regarding claim 64, Takeda discloses time-division of said time- division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel [see the entire document, including Figs. 4(A-B); Column 5, Lines 16-58].

Regarding claim 65, Takeda discloses a surplus connecting region [e.g., Fig. 2; 12, 13, & 15] that does not contribute to said display portion [e.g., Fig. 2, 11] does not occur on the said display (see the entire document, including Column 2, Line 56 - Column 3, Line 27).

Regarding claim 66, Takeda discloses said driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits [see the entire document, including Fig. 1(A)].

52. Claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** and ***Lee (US 5,426,447 A)*** as applied to claim 49 above, and further in view of ***Hirai (US 5,440,304 A)***.

Regarding claim 67, Takeda discloses said each of said plurality of driver circuits has a horizontal shift register circuit [e.g., Fig. 1(a); 31] (see the entire document, including Column 4, Lines 22-68).

Lee discloses said each of said plurality of driver circuits has a horizontal shift register circuit [e.g., Fig. 1; 49] (see the entire document, including Column 4, Line 47 - Column 5, Line 39).

Should it be shown that neither Takeda nor Lee teaches a horizontal shift register circuit with sufficient specificity; Hirai discloses a liquid crystal display [e.g., Fig. 1, 26] comprising:

a display portion [e.g., Fig. 1, 26], said display portion having a plurality of gate lines, a plurality of signal lines [e.g., Figs. 3 & 5, Y_1-Y_{80}], and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [e.g., Fig. 1; 18 and Figs. 3-5, 20], each of said plurality of driver circuits having a plurality of driver circuit output terminals [e.g., Fig. 1, Y_1-Y_{80} and Figs. 3 & 5, Y_1-Y_{80} and Fig. 4, Y_1-Y_{72}],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits (see the entire document, including Figs. 1, 4, 5), and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (see the entire document, including Column 1, Line 5 - Column 2, Line 60); wherein

said each of said plurality of driver circuits has a horizontal shift register circuit [e.g., Figs. 1 & 2; 11 and Fig. 3; 21] (see the entire document, including Column 4, Line 15 - Column 5, Line 42).

Takeda, Lee, and Hirai are analogous art, because they are from the shared inventive field of using shift register circuitry to drive liquid crystal displays. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Hirai's integrated shift register circuitry to drive Lee and Takeda's combined liquid crystal display device, so as to use a conventional type of shift register and to eliminate the need for mixing serial data to be input with dummy data even if the necessary total of output bits cannot be divided by the number of output bits of a single IC.

It would have been obvious to one of ordinary skill in the art at the time of invention because all the claimed elements were known in the prior art and one skilled in the art could have combined the integrated shift register circuitry as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known shift register circuit for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the technique for improving (by integrating the shift register circuitry) this particular class of LCD device was part of the ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

It would have been obvious to one of ordinary skill in the art at the time of invention, because this particular known shift register circuitry integration technique was recognized as part of the ordinary capabilities of one skilled in the art.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (e.g., integrating shift register circuitry). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

It would have been obvious to one of ordinary skill in the art at the time of invention, because design incentives or market forces provided a reason to make a shift register circuitry integration adaptation, and the invention resulted from application of the prior knowledge in a predictable manner.

Regarding claim 68, Hirai discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal

shift register circuit of said plurality of driver circuits (see the entire document, including Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 69, Hirai discloses said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (see the entire document, including Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42).

Regarding claim 70, Hirai discloses said horizontal shift register circuit has sampling switches [e.g., Fig. 2, FF1-FF80], a level shifter [e.g., Fig. 1, 23], a data latch circuit [e.g., Fig. 1, 22], and a digital/analog converting circuit [e.g., Fig. 1, 22] (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Should it be shown that Hirai neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Claim Rejections - 35 USC § 102

53. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

54. Claim 49 is rejected under 35 U.S.C. 102(b) as being anticipated by ***Hayashi et al (US 4,745,406 A)***.

Regarding claim 49, Hayashi discloses a liquid crystal display (see the entire document, including the Abstract) comprising:

a display portion [e.g., Fig. 8; P], said display portion having a plurality of gate lines [e.g., Fig. 8, G], a plurality of signal lines [e.g., Fig. 1, L] and a plurality of pixels [e.g., Fig. 8; P],

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [e.g., Fig. 8; 2 & 11], each of said plurality of driver circuits having a plurality of driver circuit output terminals [e.g., Fig. 8, 13R, 13G, 13B, 12, Ms],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (see the entire document, including Column 4, Line 43 - Column 5, Line 8).

Claim Rejections - 35 USC § 103

55. Claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hayashi et al (US 4,745,406 A)*** in view of ***Hirai (US 5,440,304 A)***.

Regarding claim 67, Hayashi discloses said each of said plurality of driver circuits has a horizontal shift register circuit [e.g., Fig. 8; 2] (see the entire document, including Column 4, Line 43 - Column 5, Line 8).

Should it be shown that Hayashi neglects teaching a horizontal shift register circuit with sufficient specificity; Hirai discloses a liquid crystal display [e.g., Fig. 1, 26] comprising:

a display portion [e.g., Fig. 1, 26], said display portion having a plurality of gate lines, a plurality of signal lines [e.g., Figs. 3 & 5, Y_1-Y_{80}], and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [e.g., Fig. 1; 18 and Figs. 3-5, 20], each of said plurality of driver circuits having a plurality of driver circuit output terminals [e.g., Fig. 1, Y_1-Y_{80} and Figs. 3 & 5, Y_1-Y_{80} and Fig. 4, Y_1-Y_{72}],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits (see the entire document, including Figs. 1, 4, 5), and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (see the entire document, including Column 1, Line 5 - Column 2, Line 60); wherein

said each of said plurality of driver circuits has a horizontal shift register circuit [e.g., Figs. 1 & 2; 11 and Fig. 3; 21] (see the entire document, including Column 4, Line 15 - Column 5, Line 42).

Hayashi and Hirai are analogous art, because they are from the shared inventive field of using shift register circuitry to drive liquid crystal displays. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Hirai's integrated shift register circuitry to drive Hayashi's liquid crystal display device, so as to use a conventional type of shift register and to eliminate the need for mixing serial data to be input with dummy data even if the necessary total of output bits cannot be divided by the number of output bits of a single IC.

It would have been obvious to one of ordinary skill in the art at the time of invention because all the claimed elements were known in the prior art and one skilled in the art could have combined the integrated shift register circuitry as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known shift register circuit for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the technique for improving (by integrating the shift register circuitry) this particular class of LCD device was part of the ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

It would have been obvious to one of ordinary skill in the art at the time of invention, because this particular known shift register circuitry integration technique was recognized as part of the ordinary capabilities of one skilled in the art.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (e.g., integrating shift register circuitry). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

It would have been obvious to one of ordinary skill in the art at the time of invention, because design incentives or market forces provided a reason to make a shift register circuitry integration adaptation, and the invention resulted from application of the prior knowledge in a predictable manner.

Regarding claim 68, Hirai discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (see the entire document, including Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 69, Hirai discloses said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (see the entire document, including Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42).

Regarding claim 70, Hirai discloses said horizontal shift register circuit has sampling switches [e.g., Fig. 2, FF1-FF80], a level shifter [e.g., Fig. 1, 23], a data latch circuit [e.g., Fig. 1, 22], and a digital/analog converting circuit [e.g., Fig. 1, 22] (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Should it be shown that Hirai neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Claim Rejections - 35 USC § 102/103

56. Claims 67-70 are rejected under 35 U.S.C. 102(b) as anticipated by ***Hirai (US 5,440,304 A)***.

57. Or, in the alternative, claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hirai (US 5,440,304 A)***.

Regarding claim 67, Hirai discloses a liquid crystal display [e.g., Fig. 1, 26] comprising:

a display portion [e.g., Fig. 1, 26], said display portion having a plurality of gate lines, a plurality of signal lines [e.g., Figs. 3 & 5, Y_1-Y_{80}], and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [e.g., Fig. 1; 18 and Figs. 3-5, 20], each of said plurality of driver circuits having a plurality of driver circuit output terminals [e.g., Fig. 1, Y_1-Y_{80} and Figs. 3 & 5, Y_1-Y_{80} and Fig. 4, Y_1-Y_{72}],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits (see the entire document, including Figs. 1, 4, 5), and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (see the entire document, including Column 1, Line 5 - Column 2, Line 60); wherein

said each of said plurality of driver circuits has a horizontal shift register circuit [e.g., Figs. 1 & 2; 11 and Fig. 3; 21] (see the entire document, including Column 4, Line 15 - Column 5, Line 42).

Should it be shown that Hirai neglects teaching a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate such an active matrix type structure, so as to provide a light weight display having very good image quality, wide color gamut, and relatively fast response time.

Regarding claim 68, Hirai discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (see the entire document, including Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60).

Regarding claim 69, Hirai discloses said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (see the entire document, including Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42).

Regarding claim 70, Hirai discloses said horizontal shift register circuit has sampling switches [e.g., Fig. 2, FF1-FF80], a level shifter [e.g., Fig. 1, 23], a data latch circuit [e.g., Fig. 1, 22], and a digital/analog converting circuit [e.g., Fig. 1, 22] (see the entire document, including Column 4, Line 22 - Column 5, Line 42).

Should it be shown that Hirai neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Response to Arguments

58. Applicant's arguments filed 26 October 2007 have been fully considered but they are not persuasive.

The Applicant states, "*The Office Action contends that Takeda teaches the presence of signal lines 11-b (Office Action at page 8). The Office Action further contends that Takeda teaches the presence of signal lines Q1, QN (Office Action at page 9). Clarification of what within Takeda is intended to be the signal line is respectfully requested*" (see page 17 of the reply filed 26 October 2007).

The examiner respectfully clarifies that Takeda's column electrodes [e.g., Fig. 2; 11-b] are electrically connected to the column electrodes [e.g., Fig. 1(A); Q_1-Q_N]. These column electrodes are one and the same.

The Applicant alleges, "*Takeda fails to disclose, teach, or suggest the quantity of the alleged driver circuits q1-qN being defined as N/n, wherein 'N' is the quantity of the alleged signal lines 11-b, Q1, QN and 'n' is the quantity of the alleged driver circuit output terminals 37. Lee - Lee fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein 'N' is the quantity of said signal lines and 'n' is said quantity of said driver circuit output terminals. Hayashi - Hayashi fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein 'N' is the quantity of said signal lines and 'n' is said quantity of said driver circuit output terminals*" (see pages 17-18 of the reply filed 26 October 2007). However, the examiner respectfully disagrees.

For instance, in one non-limiting example, Takeda discloses the quantity [e.g., 2] of said driver circuits [e.g., Figs. 1(A); "the first driver circuit" = (q_1 and q_2) and "the second driver circuit" = (q_3 and q_4)] being defined as N/n, wherein "N" is the quantity [e.g., 4] of said signal

lines [e.g., Fig. 1(A); Q_1, Q_2, Q_3, and Q_4] and "n" is said quantity [e.g., 2] of said driver circuit output terminals [e.g., Figs. 1(A); wherein "the first driver circuit" = (q_1 and q_2) has two output terminals at 36-1 and 36-2; and "the second driver circuit" = (q_3 and q_4) has two output terminals at 36-3 and 36-4] (see the entire document, including Column 4, Lines 22-68).

For instance, in another non-limiting example, Hayashi discloses the quantity [e.g., 2] of said driver circuits [e.g., Fig. 8; "the first driver circuit" = (M_1 and M_2) and "the second driver circuit" = (M_3 and M_4)] being defined as N/n, wherein "N" is the quantity [e.g., 4] of said signal lines [e.g., Fig. 8; Columns 1-4 driven by transistors M_{1-4}] and "n" is said quantity [e.g., 2] of said driver circuit output terminals [e.g., Fig. 8; wherein "the first driver circuit" = (M_1 and M_2) has two output terminals driving the first two column electrodes; and "the second driver circuit" = (M_3 and M_4) has two output terminals driving the second two column electrodes] (see the entire document, including Column 4, Line 43 - Column 5, Line 8).

The Applicant alleges, "*Takeda fails to disclose, teach, or suggest the quantity of gate circuits 37 being set to a power of 2. Lee - Lee fails to disclose, teach, or suggest a quantity of driver circuit output terminals being set to a power of 2. Hayashi - Hayashi fails to disclose, teach, or suggest a quantity of driver circuit output terminals being set to a power of 2*" (see pages 18-19 of the reply filed 26 October 2007). However, the examiner respectfully disagrees.

Takeda discloses the quantity [e.g., 2] of driver circuit output terminals [e.g., Figs. 1(A); wherein "the first driver circuit" = (q_1 and q_2) has two output terminals at 36-1 and 36-2; and "the

second driver circuit" = (q_3 and q_4) has two output terminals at 36-3 and 36-4] being set to a power of 2 (see the entire document, including Column 4, Lines 22-68).

Hayashi discloses the quantity [e.g., 2] of driver circuit output terminals [e.g., Fig. 8; wherein "the first driver circuit" = (M_1 and M_2) has two output terminals driving the first two column electrodes; and "the second driver circuit" = (M_3 and M_4) has two output terminals driving the second two column electrodes] being set to a power of 2 (see the entire document, including Column 4, Line 43 - Column 5, Line 8).

Applicant's arguments with respect to claims 25-29, 31, 37, 43-48, and 67-78 have been considered but are moot in view of the new grounds of rejection.

Claims 49-66 were left unamended by the Applicant. The grounds of rejection for these claims are unchanged relative to the immediate previous office action.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

59. The detailed rejections (linking instantly claimed subject matter to particular prior art teachings) above are merely examplary in nature. The instant claims are so exceedingly broadly worded that one having ordinary skill in the art would reasonably construe multiple

interpretations and readings of the instant invention's scope. Moreover, many pending claims are so thoroughly indefinite that a near infinite number of scope interpretations result. The examiner has attempted to provide examples of how an artisan would consider particular prior art embodiments as reading on the instant invention. However, these examples do not and should be considered to limit other prior art embodiment teachings from reading on the instantly claimed invention equally well. The examiner reserves the right to cite other prior teaching embodiments and examples from the references relied upon above to more fully explain how the grounds of rejection read on the instantly claimed invention. The Applicant is respectfully reminded the grounds of rejection are the referenced documents in their entirety, not simply the small examplary portions that the examiner has pointed to. If the examiner listed every possible embodiment example taught by the prior art which reads on the instant invention, this office action would be hundreds of pages in length.

60. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
20 May 2008